Switching Control of Buck Converter Based on Energy Conservation Principle

L. Wang, Q. H. Wu, *Fellow, IEEE*, Y. K. Tao, and W. H. Tang, *Senior Member, IEEE*

***Abstract*— This brief presents a switching control scheme (SCS) based on the energy conservation principle for buck converters. The concept of the SCS is based on the conservation of energy in circuit. It keeps the balance between the energy that is injected into a circuit and the sum of the energy that is consumed by the load and stored in reactive components. The SCS not only regulates the output voltage of the buck converter accurately under static conditions, but also improves its dynamic responses to disturbances of input voltage and load current. Furthermore, the SCS is capable of operating in both the continuous current mode and the discontinuous current mode, and the stability analysis undertaken using the Lyapunov stability criterion shows that the SCS is stable in all cases. Simulation and experimental results confirm the possibility and attractiveness of using this method to control buck converters.**

***Index Terms*— Buck converter, dynamic response, energy conservation principle, stability analysis, switching control.**

I. Introduction

With the development of microelectronics and power electronics, dc–dc converters are widely used. In addition, as the voltage regulation criteria for digital circuit's supply voltage become more stringent, there is an increasing demand for high dynamic performance power converters. Until now, PID controllers are still one of the most commonly used control methods for converters. However, the PID control systems suffer from the limitations of slow compensator networks, which lead to poor dynamic performances of converters [1].

As control methods play an important role on improving the dynamic performance of converters, various control methods have been proposed to provide improved dynamic performances. The hysteresis control, as presented in [2]–[4], provides fast dynamic responses, since the conventional feedback compensation network is removed. However, the drawbacks of this method are its variable switching frequency and nonzero steady-state error. Sliding-mode control (SMC) is one of the effective non-linear robust control approaches, since it provides system dynamics with an invariance property to uncertainties once the system dynamics are controlled in the sliding mode [5]–[7]. However, there are some problems to be solved, such as chattering phenomena and nonconstant switching frequency, when conventional SMC is used in the power converters. As another typical nonlinear control strategy, the one-cycle control (OCC) has been studied for decades [8], [9]. While its inhibitory capability to variations of input voltage is satisfactory, the inhibitory capability to load changes is still poor. Recently, in [10]–[12], a control algorithm based on the principle of capacitor charge balance has been studied for dc–dc converters to achieve optimal dynamic performance under load current changes. However, the accurate calculation of the duty-ratio required by this control algorithm is difficult to achieve.

An ideal buck controller would behave linearly during steady-state conditions for tight voltage regulation and nonlinearly during transient conditions for fast response. It is demonstrated in [12]–[14] that by employing two separate controllers for steady-state operation and for transient operation, the dynamic response can be improved while not sacrificing the steady-state accuracy. However, the accurate detection of the time when disturbances occur is not easy. In [15], a hybrid mode-switched control scheme that uses energy balance principle to calculate the reference voltage and current has been proposed for dc–dc converters. With this scheme, the dynamic performances of the converters are improved. However, the main drawback of this scheme is that it is designed based on working in DCM. Under CCM, the reference current is difficult to calculate, since not all the energy stored by the inductor is transferred to the load in one switching cycle.

In our research, an SCS based on the energy conservation principle is proposed to control buck converters. This brief is organized as follows. In Section II, the SCS is designed. Section III illustrates the implementation procedures of the SCS, including the computation of the energy that the inductor stores. The stability analysis of the SCS is studied in Section IV, and the dynamic response is analyzed in Section V. Simulation and experimental results are presented in Section VI, and the conclusions are presented in Section VII.

II. Derivation of the Switching Controller

The structure of a buck converter is shown in Fig. 1, where i_ℓ represents the current of inductor L, i_o represents the current of the load R, and u_o represents the output voltage. For the buck converter, the energy conservation in the circuit is expressed as follows:

$$W_\mathrm{in}(n) = W_\mathrm{out}(n) + \Delta W_\ell(n) + \Delta W_\mathrm{c}(n) + W_\mathrm{s}(n) \quad (n = 1, 2 \ldots) \quad (1)$$

Manuscript received July 15, 2015; accepted November 21, 2015. Manuscript received in final form November 25, 2015. This work was supported in part by the Guangdong Innovative Research Team Program, China, under Grant 201001N0104744201 and in part by the State Key Program of National Natural Science of China under Grant 51437006. Recommended by Associate Editor Q.-C. Zhong. *(Corresponding author: Q. H. Wu.)*

L. Wang, Y. K. Tao, and W. H. Tang are with the School of Electric Power Engineering, South China University of Technology, Guangzhou 510641, China (e-mail: w.lei19@mail.scut.edu.cn; taoyukun@mail.scut.edu.cn; wenhutang@scut.edu.cn).

Q. H. Wu is with the School of Electric Power Engineering, South China University of Technology, Guangzhou 510641, China, and also with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3GJ, U.K. (e-mail: wuqh@scut.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCST.2015.2505625

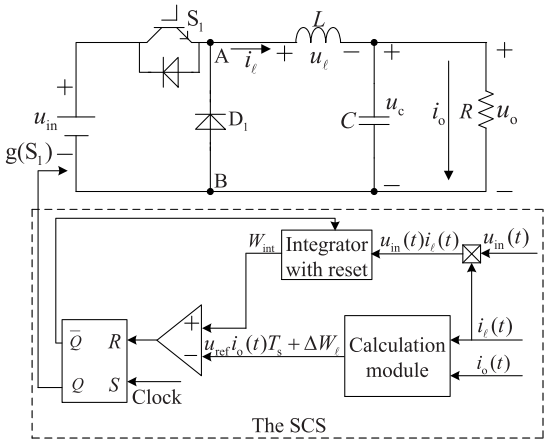


Fig. 1. Structure of a buck converter with the SCS.

it means that, during the nth switching cycle $[(n-1)T_s, nT_s)$, the energy that is injected into the circuit $W_{in}(n)$ should be equal to the sum of the output energy $W_{out}(n)$, the energy that the reactive components (L and C) store ($\Delta W_c(n) + \Delta W_\ell(n)$), and the conduction losses of the switch and the diode $W_s(n)$.

The following proves that $\Delta W_c(n)$ in (1) can be ignored. First, the output voltage u_o and capacitor voltage u_c are different due to the equivalent series resistance (ESR) of the capacitor, but if the ESR is negligible, then we can assume that u_c is equal to u_o. Then compared with the average output voltage, the output voltage ripple is negligible. And as our purpose is to ensure that u_o is always equal to the reference voltage u_{ref}, which is a constant value, u_o can be substituted by u_{ref}. The above assumptions give

$$u_c(t) = u_o(t) = u_{ref}. \tag{2}$$

And the energy the capacitor stores is calculated using

$$\Delta W_c(t) = \int_{(n-1)T_s}^{t} u_c(t) i_c(t) dt \quad (t \in [(n-1)T_s, nT_s)). \tag{3}$$

As the capacitor C works the entire cycle during each switching cycle n, $\Delta W_c(n)$ is calculated in

$$\Delta W_c(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} u_c(t) i_c(t) dt \tag{4}$$

where $i_c(t)$ represents the capacitor current, which is calculated in

$$i_c(t) = C\frac{du_c(t)}{dt}. \tag{5}$$

Based on (2), $\Delta W_c(n)$ can be obtained as

$$i_c(t) = C\frac{du_c(t)}{dt} = C\frac{du_{ref}}{dt} = 0 \Rightarrow \Delta W_c(n) = 0. \tag{6}$$

Thus $W_c(n)$ in (1) can be ignored, and then the energy conservation in the circuit can be rewritten as follows:

$$W_{in}(n) = W_{out}(n) + \Delta W_\ell(n) + W_s(n) \quad (n = 1, 2, 3 \ldots). \tag{7}$$

After obtaining (7), W_{in}, W_{out}, ΔW_ℓ and W_s of the buck converter working in CCM and DCM are calculated though the state analysis in the following of this section, respectively.

A. Continuous Conduction Mode

Under the CCM operation mode, the buck converter operates in two states: 1) state 1—switch S_1 is ON and 2) state 2—S_1 is OFF. Thus, during the nth switching cycle, we have

$$t_{ON}(n) + t_{OFF}(n) = T_s \quad (n = 1, 2, 3 \ldots) \tag{8}$$

where $t_{ON}(n)$ and $t_{OFF}(n)$ represent the opening and closing durations of S_1, respectively.

State 1: when S_1 is ON, energy is injected into the circuit, and i_ℓ flows through the loop ($u_{in} \rightarrow S_1 \rightarrow L \rightarrow C \parallel R \rightarrow u_{in}$). In this switching state, L is charged, and S_1 and R consume energy, and u_{AB} is obtained using

$$u_{AB}(t) = u_{in}(t) - u_{sat} \quad (t \in [(n-1)T_s, (n-1)T_s + t_{ON}(n))) \tag{9}$$

where u_{sat} represents the ON-state voltage drop of S_1.

State 2: when S_1 is OFF, no energy is fed into the circuit, however, i_ℓ continues flowing through the loop ($D_1 \rightarrow L \rightarrow C \parallel R \rightarrow D_1$). In this switching state, L is discharged, and D_1 and R consume energy, and u_{AB} is obtained using

$$u_{AB}(t) = -u_d \quad (t \in [(n-1)T_s + t_{ON}(n), nT_s)) \tag{10}$$

where u_d represents the ON-state voltage drop of the diode D_1.

The above state analysis shows that the voltage source works in the time interval from $(n-1)T_s$ to $(n-1)T_s + t_{ON}(n)$, while L and R work in the entire switching cycle. Thus, the values of $W_{in}(n)$, $W_{out}(n)$, $\Delta W_\ell(n)$, and $W_s(n)$ during the nth switching cycle can be obtained as follows:

$$W_{in}(n) = \int_{(n-1)T_s}^{(n-1)T_s+t_{ON}(n)} u_{in}(t) i_\ell(t) dt \tag{11}$$

$$W_{out}(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} u_o(t) i_o(t) dt \tag{12}$$

as $u_o = u_{ref}$ from (2), (12) becomes

$$W_{out}(n) = u_{ref} i_o(t) T_s \tag{13}$$

$\Delta W_\ell(n)$ and $W_s(n)$ are calculated as follows:

$$\Delta W_\ell(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} u_\ell(t) i_\ell(t) dt \tag{14}$$

$$W_s(n) = \int_{(n-1)T_s}^{(n-1)T_s+t_{ON}(n)} U_{sat} i_\ell(t) dt + \int_{(n-1)T_s+t_{ON}(n)}^{nT_s} u_d i_\ell(t) dt. \tag{15}$$

Substituting the values of $W_{in}(n)$, $W_{out}(n)$, $\Delta W_\ell(n)$, and $W_s(n)$ calculated above into (7), the energy conservation is rewritten as follows after adjusting:

$$\int_{(n-1)T_s}^{(n-1)T_s+t_{ON}(n)} (u_{in}(t) - u_{sat}) i_\ell(t) dt + \int_{(n-1)T_s+t_{ON}(n)}^{nT_s} -u_d dt = u_{ref} i_o(t) T_s + \int_{(n-1)T_s}^{nT_s} u_\ell(t) i_\ell(t) dt \quad (n = 1, 2 \ldots). \tag{16}$$

B. Discontinuous Conduction Mode

Under the DCM operation mode, the buck converter operates in three states, in which switch S_1 is ON for a duration of $t_{ON}(n)$ and is OFF for durations $t_{OFF1}(n)$ and $t_{OFF2}(n)$, and $t_{ON}(n)+t_{OFF1}(n)+t_{OFF2}=T_s(n)$.

State 1: when S_1 is on, energy is injected into the circuit, and i_ℓ flows through the loop ($u_{in} \rightarrow S_1 \rightarrow L \rightarrow C \parallel R \rightarrow u_{in}$). In this switching state, L is charged, and S_1 and R consume energy, and u_{AB} is obtained using

$$u_{AB}(t)=u_{in}(t)-u_{sat} \quad (t \in [(n-1)T_s, (n-1)T_s+t_{ON}(n))). \tag{17}$$

State 2: when S_1 is OFF, no energy is fed into the circuit. Energy stored in L is discharged through the loop ($D_1 \rightarrow L \rightarrow C \parallel R \rightarrow D_1$). In this switching state, L is discharged, and D_1 and R consume energy. u_{AB} is obtained in

$$u_{AB}(t) = -u_d(t \in [(n-1)T_s + t_{ON}(n), (n-1)T_s + t_{ON}(n) + t_{OFF1}(n))). \tag{18}$$

State 3: when S_1 is still OFF and energy stored in L is discharged out, $i_\ell = 0$. However, the load still consumes energy from the capacitor. In this switching state, R consumes energy, and u_{AB} is obtained using

$$u_{AB}(t) = 0 \quad (t \in [(n-1)T_s + t_{ON}(n) + t_{OFF1}(n), nT_s)). \tag{19}$$

By combining state 1, state 2, and state 3, $W_{in}(n)$, $W_{out}(n)$, $\Delta W_\ell(n)$, and $W_s(n)$ under DCM can be calculated similarly to that of the CCM operation mode. Then substituting these calculated values into (7), we get

$$\begin{aligned}&\int_{(n-1)T_s}^{(n-1)T_s+t_{ON}(n)} (u_{in}(t)-u_{sat})i_\ell(t)dt \\ &\quad + \int_{(n-1)T_s+t_{ON}(n)}^{(n-1)T_s+t_{ON}(n)+t_{OFF1}(n)} -u_d i_\ell(t)dt \\ &\quad + \int_{(n-1)T_s+t_{ON}(n)+t_{OFF1}(n)}^{nT_s} 0 i_\ell(t)dt \\ &= u_{ref} i_o(t) T_s + \int_{(n-1)T_s}^{nT_s} u_\ell(t) i_\ell(t) dt \quad (n=1,2\ldots).\end{aligned} \tag{20}$$

Equations (16) and (20) are the main equations that the duration $t_{ON}(n)$ and $t_{OFF}(n)$ must satisfy during each switching cycle to implement the SCS. Combining the aforementioned state analysis, it is observed that (16) and (20) can both be realized by controlling the switching variable u_{AB}, which is expressed in

$$\begin{aligned}&\int_{(n-1)T_s}^{nT_s} u_{AB}(t) i_\ell(t) dt \\ &= u_{ref} i_o(t) T_s + \int_{(n-1)T_s}^{nT_s} u_\ell(t) i_\ell(t) dt \quad (n=1,2\ldots).\end{aligned} \tag{21}$$

III. Implementation of the SCS

A. Calculation of the Control Reference $W_{out}(n)+\Delta W_\ell(n)$

As control reference, $W_{out}(n) + \Delta W_\ell(n)$ should be calculated in the time instant of the beginning of the nth switching cycle and kept during the entire switching cycle. After measuring the variable i_o, $W_{out}(n)$ is obtained by (13). And as we know, the energy is absorbed and released equally by the inductor in a switching cycle under the steady-state conditions. However, it is not equal under the dynamic state conditions, since the inductor current cannot change instantaneously. Therefore, to ensure the dynamic performances, $\Delta W_\ell(n)$ should be considered and calculated as follows:

$$\Delta W_\ell(t) = \int_{(n-1)T_s}^{t} u_\ell(t) i_\ell(t) dt \quad (t \in [(n-1)T_s, (n-1)T_s+T_s)) \tag{22}$$

where i_ℓ is the measured variable, and u_ℓ is obtained using

$$u_\ell(t) = L\frac{i_\ell(t+T_c) - i_\ell(t)}{T_c} \tag{23}$$

where T_c is the sampling cycle.

The state analysis shows that the inductor works during the entire switching cycle, which means the time t of (22) goes to the end of the nth switching cycle, therefore, $\Delta W_\ell(n)$ is calculated by (14). Note here that the control reference is collected only in the time instant of the beginning of each switching cycle, therefore, $\Delta W_\ell(n)$ used in the control reference of the nth switching cycle is actually $\Delta W_\ell(n-1)$ calculated in the $(n-1)$th switching cycle, which means $\Delta W_\ell(n)$ used in the SCS has a switching cycle lag.

B. Implementation Procedure of the SCS

After the computation of $W_{out}(n) + \Delta W_\ell(n)$, the SCS can be implemented with simple logic functions (comparison and integration) as shown in Fig. 1. Here, the implementation for control of a CCM buck converter is described as follows: the integration process starts at the moment when S_1 is turned ON by the fixed frequency clock pulse. At this moment, $u_{AB}(t) = u_{in}(t) - u_{sat}$. As time goes on, the integration value $W_{int}(t)$ increases from its initial value shown in Fig. 2 as follows:

$$\begin{aligned}W_{int}(t) = &\int_{(n-1)T_s}^{t} (u_{in}(t)-u_{sat}) i_\ell(t) dt \\ &+ W_{initial}(n) \quad (t \in [(n-1)T_s, (n-1)T_s+T_s))\end{aligned} \tag{24}$$

and $W_{int}(t)$ compares with $W_{out}(n)+\Delta W_\ell(n)$ instantaneously. At the instance when $W_{int}(t)$ reaches $W_{out}(n) + \Delta W_\ell(n)$, the comparator generates a reset pulse to reset the RS flip-flop to be ($Q = 0$). Then switch S_1 is changed from the ON-state to the OFF-state. At the same time, the integrator is reset to zero. t at this moment is defined as $(n-1)T_s + d_{SCS}(n)T_s$ of the present cycle n, which is determined by the following equation:

$$\begin{aligned}&W_{initial}(n) + \int_{(n-1)T_s}^{(n-1)T_s+d_{SCS}(n)T_s} (u_{in}(t)-u_{sat}) i_\ell(t) dt \\ &\quad = W_{out}(n) + \Delta W_\ell(n) = u_{ref} i_o(t) T_s + \Delta W_\ell(n)\end{aligned} \tag{25}$$

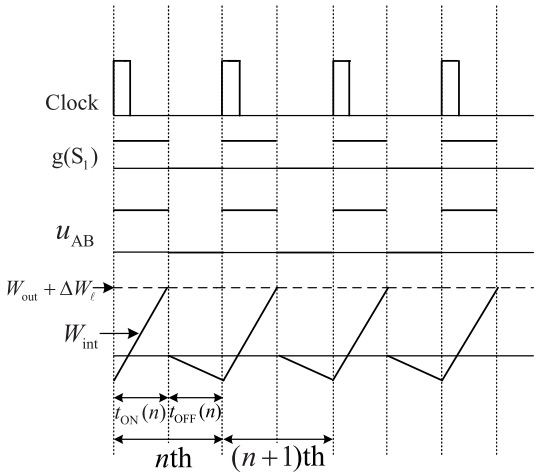


Fig. 2. Operation waveform of the SCS of the buck converter.

where $d_{\mathrm{SCS}}(n)$ is the duty ratio, which is $t_{\mathrm{ON}}(n)/T_{\mathrm{s}}$, and $W_{\mathrm{initial}}(n)$ is the integration value during the OFF-state of S_1, in this switching state, no energy is injected into the circuit, and u_{AB} is equal to $-u_{\mathrm{d}}$. Then the integration restarts from zero with the value of $-u_{\mathrm{d}} i_\ell(t)$ after the reset, as shown in Fig. 2. The switch S_1 is OFF until the arrival of the next clock pulse, which starts the $(n+1)$th switching cycle. Thus

$$W_{\mathrm{initial}}(n) = \int_{(n-1)T_{\mathrm{s}}+d_{\mathrm{SCS}}(n)T_{\mathrm{s}}}^{nT_{\mathrm{s}}} -u_{\mathrm{d}} i_\ell(t)dt. \tag{26}$$

As the implementation for a DCM buck converter is similar to that of CCM, the details are not presented here.

IV. Steady-State Analysis

A. Steady-State Operation Analysis

Under the steady-state conditions, the inductor absorbs and releases equal energy, which means $\Delta W_\ell(t) = 0$. Meanwhile, after reaching the steady state, $i_\ell(t)$ is equal to $i_o(t)$ by neglecting the current ripple. Thus, (21) becomes

$$\frac{1}{T_{\mathrm{s}}} \int_{(n-1)T_{\mathrm{s}}}^{(n-1)T_{\mathrm{s}}+T_{\mathrm{s}}} u_{\mathrm{AB}}(t)dt = u_{\mathrm{ref}} \tag{27}$$

from (21), it is observed that in each switching cycle, the average of the switching variable $u_{\mathrm{AB}}(t)$ is exactly equal to the control reference u_{ref}, which ensures the tracking of the output voltage to u_{ref} in each switching cycle [8].

B. Stability Analysis

Under the steady state, neglecting $\Delta W_\ell(t)$ since $\Delta W_\ell(t) = 0$ and the conduction losses of S_1 and D_1, (25) becomes

$$\frac{1}{T_{\mathrm{s}}} \int_{(n-1)T_{\mathrm{s}}}^{(n-1)T_{\mathrm{s}}+d_{\mathrm{SCS}}(n)T_{\mathrm{s}}} u_{\mathrm{in}}(t) i_\ell(t)dt = u_{\mathrm{ref}} i_{\mathrm{o}}(t)$$

$$\Longrightarrow d_{\mathrm{SCS}}(n) = \frac{u_{\mathrm{ref}} i_{\mathrm{o}}(t)}{u_{\mathrm{in}}(t) i_\ell(t)}. \tag{28}$$

Then a buck converter with the SCS can be described by the following system of differential equations:

$$\begin{aligned} \dot{x}(t) &= Ax(t) + Bu_{\mathrm{in}}(t) \\ d_{\mathrm{SCS}} &= \frac{u_{\mathrm{ref}} i_o(t)}{u_{\mathrm{in}}(t) i_\ell(t)} \end{aligned} \tag{29}$$

where

$$x(t) = \begin{bmatrix} i_\ell(t) \\ u_{\mathrm{o}}(t) \end{bmatrix}, \quad A = \begin{bmatrix} -\dfrac{R_\ell}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix}, \quad B = \begin{bmatrix} \dfrac{d_{\mathrm{SCS}}}{L} \\ 0 \end{bmatrix}$$

and R_ℓ represents the parasitic resistance of the inductor (for simplicity, the parasitic resistance of C was neglected).

A disturbance to the converter causes the changes $\widehat{u}_{\mathrm{o}}(t)$ in the output voltage, $\widehat{i}_\ell(t)$ in the inductor current, and $\widehat{d}_{\mathrm{SCS}}$ in the duty ratio.

System (29) can be rewritten in terms of disturbances

$$\begin{aligned} \dot{\widehat{x}}(t) &= A\widehat{x}(t) + B_1 V_{\mathrm{in}} \\ \widehat{d}_{\mathrm{SCS}} &= \frac{V_{\mathrm{ref}}}{R V_{\mathrm{in}} I_\ell} \widehat{u}_{\mathrm{o}}(t) - \frac{D}{I_\ell} \widehat{i}_\ell(t) \end{aligned} \tag{30}$$

where $\widehat{x}(t) = \begin{bmatrix} \widehat{i}_\ell(t) \\ \widehat{u}_{\mathrm{o}}(t) \end{bmatrix}$, $B_1 = \begin{bmatrix} \dfrac{\widehat{d}_{\mathrm{SCS}}}{L} \\ 0 \end{bmatrix}$, and V_{in}, D, and I_ℓ are the steady components.

A Lyapunov function is defined as

$$V = \frac{1}{2} L \widehat{i}_\ell{}^2 + \frac{1}{2} C \widehat{u}_{\mathrm{o}}{}^2 \tag{31}$$

where $V > 0$, and the derivative of this is expressed as follows:

$$\frac{dV}{dt} = L\widehat{i}_\ell \frac{d\widehat{i}_\ell}{dt} + C\widehat{u}_{\mathrm{o}} \frac{d\widehat{u}_{\mathrm{o}}}{dt}. \tag{32}$$

By using (30) and replacing $\widehat{i}_\ell$ with $\widehat{d}_{\mathrm{SCS}}$, one gets

$$\begin{aligned} \frac{dV}{dt} &= -R\widehat{i}_\ell{}^2 - \frac{\widehat{u}_{\mathrm{o}}{}^2}{R} + V_{\mathrm{in}} \widehat{d}_{\mathrm{SCS}} \widehat{i}_\ell \\ &= -R\widehat{i}_\ell{}^2 - \frac{\widehat{u}_{\mathrm{o}}{}^2}{R} - \frac{\widehat{d}_{\mathrm{SCS}}^2 I_\ell}{D} + \frac{V_{\mathrm{ref}} \widehat{u}_{\mathrm{o}} \widehat{d}_{\mathrm{SCS}}}{RD}. \end{aligned} \tag{33}$$

In a closed-loop controlled converter, any increase in the output voltage ($\widehat{u}_{\mathrm{o}} > 0$), for a static value, causes a decrease in the duty ratio ($\widehat{d}_{\mathrm{SCS}} < 0$) to shorten the opening duration of S_1, and thus for bringing down back the output voltage to its static value and vice versa [16]. It is obvious that $((V_{\mathrm{ref}} \widehat{u}_{\mathrm{o}} \widehat{d}_{\mathrm{SCS}})/RD) < 0$, which satisfies the Lyapunov stability criterion [16], [17]. Hence, the SCS is stable.

V. Analysis of Dynamic Response

The capacitor voltage drop is reconsidered as $\Delta u_{\mathrm{c}}(n)$ here for the analysis of the transient response. Since the dynamic performance under a load current change is arguably the most important issue in power converter design, the transient response to a positive load current change will be fully discussed. Referring to Fig. 3, immediately following the load current step change $i_{\mathrm{o1}} \rightarrow i_{\mathrm{o2}}$, the inductor current cannot

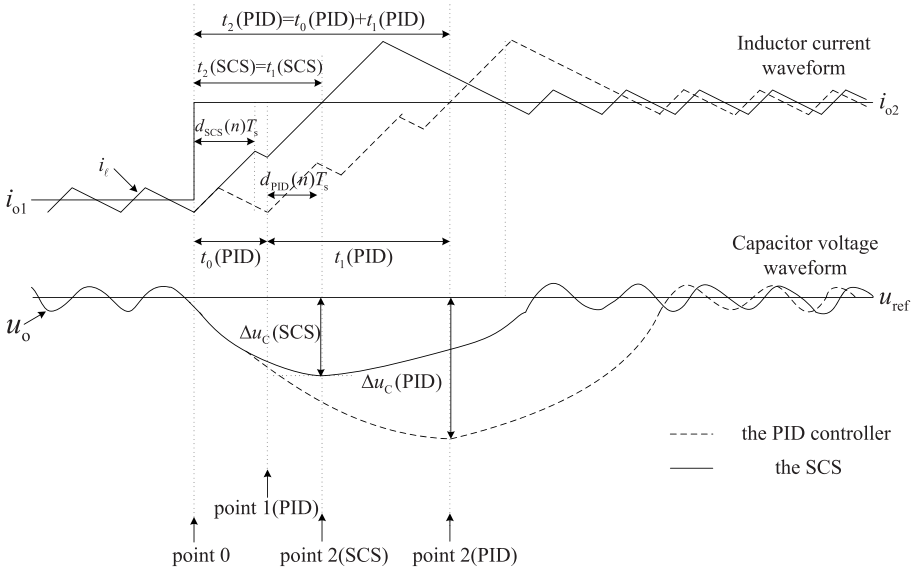


Fig. 3. Inductor current path of a buck converter under a positive load current step.

change instantaneously to supply the step of the load current. Therefore, a portion of the load current must be supplied by the output capacitor. This, in turn, causes the output capacitor to lose charge and the output voltage to decrease. Before point 2, the inductor current is lower than the load current, the capacitor voltage continues to decrease. At point 2, the inductor current is equal to the load current, and then the capacitor stops discharging. At this point, the capacitor voltage drop is at its maximum, which is expressed in

$$C\frac{du_c(t)}{dt} = i_c(t) = i_\ell(t) - i_o(t) \tag{34}$$

$$\Delta u_c(n) = \frac{1}{C}\int_{\text{Point0}}^{\text{Point2}} (i_\ell(t) - i_o(t))dt. \tag{35}$$

Assuming the positive and negative inductor slews are invariable, in order to minimize $\Delta u_c(n)$, the duration t_2, which represents the integral period (point 0–point 2), must be minimized. It means the inductor current i_ℓ should achieve the new load current as soon as possible. Here, three factors influence the inductor current to change:

1) the parameters of the circuits;
2) the delay time for responding to the disturbances;
3) the duty ratio during the increase of i_ℓ from i_{o1} to i_{o2}.

Under certain circuit parameters, the change of i_ℓ is determined by the other two factors. First, when i_o steps from i_{o1} to i_{o2}, the $t_{ON}(n)$ and $t_{OFF}(n)$ of the SCS will be immediately allocated again according to (21); at the same time, the SCS makes the corresponding adjustments immediately to the switching pulses. However, using the current-mode PID controller, the load changes are firstly responded in the inductor current. Then the switching pulse is adjusted after the changes of the inductor current get to the comparator through the compensation block. This will bring an unpredictable latency t_0, as shown in Fig. 3. Then, during the increase of Δi_ℓ based on the given Δi_o, the bigger the duty ratio is, the more quickly i_ℓ gets to i_{o2}. The following is the calculations and comparison of the duty ratios.

By neglecting the energy losses of S_1 and D_1 of (25), the duty ratio $d_{SCS}(n)$ of the SCS during t_1 (the load current has become $i_{o2}(t)$ at this time) is obtained as follows:

$$\begin{aligned}\frac{1}{T_s}\int_{(n-1)T_s}^{(n-1)T_s+d_{SCS}(n)T_s} & u_{in}(t)i_\ell(t)dt \\ &= u_{ref}i_o(t) + \frac{1}{T_s}\Delta W_\ell(n) \\ \Rightarrow d_{SCS}(n) &= \frac{u_{ref}i_{o2}(t)}{u_{in}(t)i_\ell(t)} + \frac{\Delta u_\ell(n)i_\ell(t)}{u_{in}(t)i_\ell(t)} \\ &= \frac{u_{ref}i_{o2}(t)}{u_{in}(t)i_\ell(t)} + \frac{\Delta u_\ell(n)}{u_{in}(t)}\end{aligned} \tag{36}$$

where $\Delta u_\ell(n)$ represents the average change value of the inductor voltage in the nth switching cycle.

According to the state analysis, the state average model of the buck converter is obtained as follows:

$$d(n) = \frac{L\dfrac{di_\ell(t)}{dt} + u_{ref} + \Delta u_o(t)}{u_{in}(t)}. \tag{37}$$

The designing principle of the current-mode controller is that the inner current controller is designed by ignoring the influence of the output voltage and the outer voltage controller is designed under the assumption that the actual current completely tracks the reference current. This shows that, during t_1, the purpose that the inner and outer loops adjust the duty ratio is to offset the inductor voltage changes $\Delta u_\ell(n)$, although the outer voltage loop implements this purpose by adjusting the Δu_o. Thus, according to (37), the duty ratio $d_{PID}(n)$ is obtained as follows:

$$d_{PID}(n) = \frac{u_{ref} + \Delta u_\ell(n)}{u_{in}(t)} = \frac{u_{ref}}{u_{in}(t)} + \frac{\Delta u_\ell(n)}{u_{in}(t)}. \tag{38}$$

Because $i_\ell(t) < i_{o2}(t)$ during t_1, the comparison between (36) and (38) shows that $d_{SCS}(n)$ is always greater than $d_{PID}(n)$ until i_ℓ reaches i_{o2}. Therefore, Δu_c(SCS) is smaller than Δu_c(PID), as shown in Fig. 3. Since i_ℓ using the SCS can

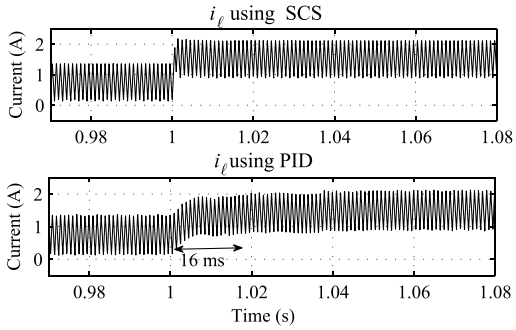


Fig. 4. Responses of the inductor current to a positive load current step.

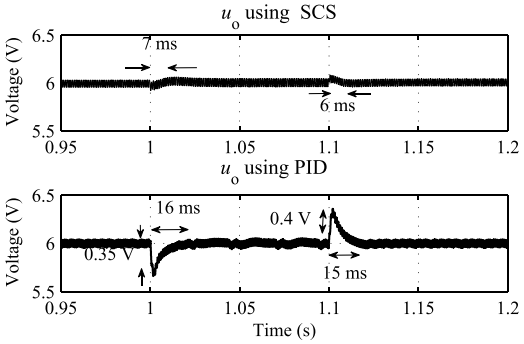


Fig. 5. Simulation results of output voltage response to the load current changes for the buck converter A working in CCM.

approach the new output current i_{o2} more quickly, the recovery time can be reduced in such a situation, as shown in Fig. 3. This is demonstrated in Fig. 4, which shows the simulation comparison results of the inductor current responses using the SCS and the PID controller to the load current step by changing the load from 8 to 4 Ω. The simulation results show that the inductor current using the SCS increases to the new steady-state output current very quickly. However, with the PID controller, the inductor current takes more than 16 ms to get to the new steady state. Under other transient conditions, the analysis is virtually similar to those detailed above.

VI. Simulation and Experimental Results

Simulation and experimental results are used to demonstrate the superior performances of the SCS. For simulation studies, buck converter A with the low switching frequency $f_s = 1$ kHz and buck converter B with the high switching frequency $f_s = 40$ kHz are configured. To evaluate the performances of the SCS, the following section presents a comparative study with a current-mode PID controller. A comparison is made with a current-mode controller because it is most frequently used in voltage regulator module (VRM) applications.

According to the circuit shown in Fig. 1, buck converter A has the parameters: $u_{in} = 15$ V, $u_{ref} = 6$ V, $\Delta u_{pp} = 0.08$ V, $R = 8$ Ω, $L = 2500$ μH (CCM)/ 800 μH (DCM), $C = 1200$ μF (CCM)/2200 μF (DCM). The inductances and capacitances are determined by the following equations:

$$L_{(\text{critical})} = \frac{u_{\text{ref}}(1-d)}{2i_{o(\min)}f_s}$$
$$C = \frac{u_{\text{ref}}(1-d)}{8\Delta u_{pp}Lf_s^2} \tag{39}$$

where $L_{(\text{critical})}$ represents the critical inductance between CCM and DCM; L represents the inductance determined according $L_{(\text{critical})}$. The PID controllers are designed by the SISO tool of MATLAB with the crossing frequency of 192 Hz and the phase margin of 50.3°.

Figs. 5–8 show the responses of buck converter A working in CCM and DCM undergoing step changes of the load current and input voltage. In Fig. 5, the responses to the load current steps of CCM buck converter A are compared with that of the PID controller. The results show that under the positive current step change by changing the load from 8 to 4 Ω, the voltage peak undershoot Δu_o is reduced from −0.35 (with the PID controller) to −0.1 V (with the SCS) and the settling time t_{settling} is reduced from 16 ms to 7 ms.

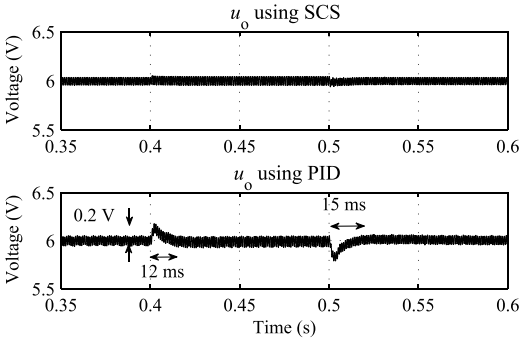


Fig. 6. Simulation results of output voltage response to the input voltage changes (15 V → 18 V → 12 V) for buck converter A working in CCM.

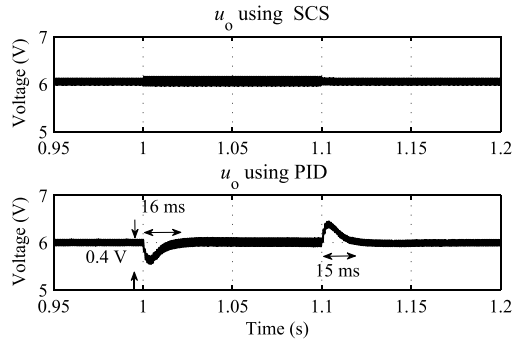


Fig. 7. Simulation results of output voltage response to the load current changes for buck converter A working in DCM.

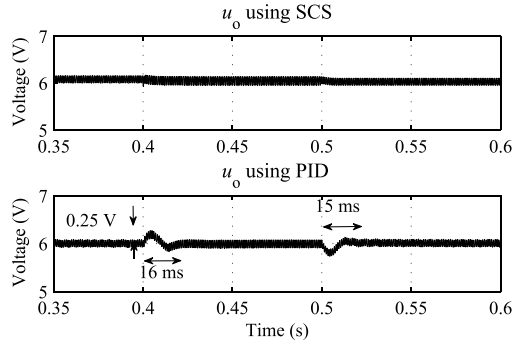


Fig. 8. Simulation results of output voltage response to the input voltage changes (15 V → 18 V → 12 V) for buck converter A working in DCM.

TABLE I
SIMULATION RESULTS OF BUCK CONVERTER A IN ALL THE DYNAMIC CASES

disturbance (R or u_{in})	SCS		PID	
	Δu_o	$t_{settling}$	Δu_o	$t_{settling}$
8 Ω → 4 Ω → 8 Ω (CCM)	-0.1 V / 0.05 V	7 ms / 6 ms	-0.35 V / 0.4 V	16 ms / 15 ms
15 V→ 18 V → 12 V (CCM)	0.02 V / -0.03 V	2 ms / 3 ms	0.2 V / -0.2 V	12 ms / 15 ms
8 Ω → 4 Ω → 8 Ω (DCM)	0 V / 0 V	0 ms / 0 ms	-0.4 V / 0.38 V	16 ms / 15 ms
15V→ 18V → 12V (DCM)	0.05 V / -0.03 V	3 ms / 2 ms	0.25 V / -0.15 V	16 ms / 15 ms

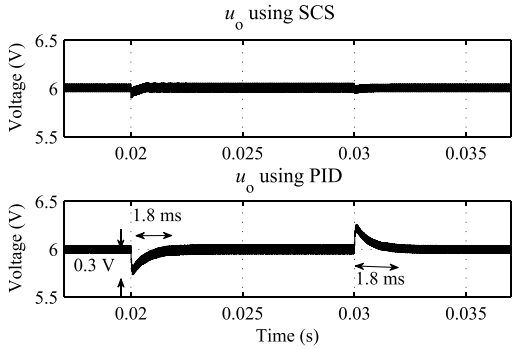


Fig. 9. Simulation results of output voltage response to the load current changes for the buck converter B working in CCM.

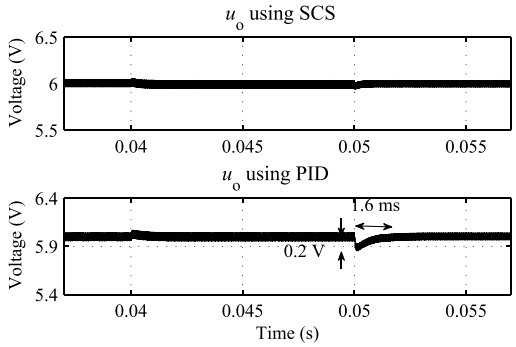


Fig. 10. Simulation results of output voltage response to the input voltage changes (15 V → 18 V → 12 V) for buck converter B working in CCM.

Table I summarizes the simulation comparison results of the responses of the SCS and the PID controller to all the dynamic cases. It is observed from Table I that, compared with the PID controller, the voltage peak shoot Δu_o and the settling time $t_{settling}$ with the SCS are significantly reduced in all cases.

In order to further verify the functionality of the SCS, a buck converter B is configured with the parameters: $u_{in} = 15$ V, $u_{ref} = 6$ V, $\Delta u_{pp} = 0.08$ V, $R = 8$ Ω, $L = 40$ μH (CCM)/20 μH (DCM), $C = 100$ μF (CCM)/ 150 μF (DCM). The PID controllers are designed by the SISO Tool of MATLAB with the crossing frequency of 6 kHz and the phase margin of 62°. Figs. 9–12 show the simulation waveforms of the buck converter B under CCM operation and DCM operation, respectively. And the comparison results of the voltage shoot and settling time are summarized in Table II. The simulation results demonstrate that the SCS still has improved dynamic performances when the switching frequency increased to 40 kHz.

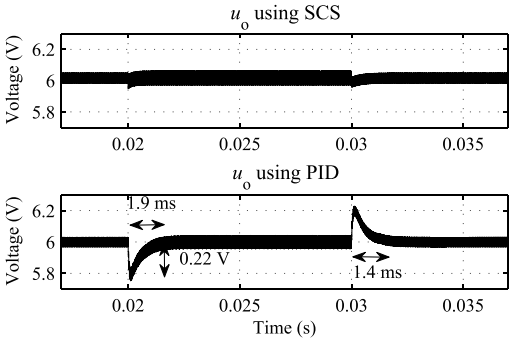


Fig. 11. Simulation results of output voltage response to the load current changes for buck converter B working in DCM.

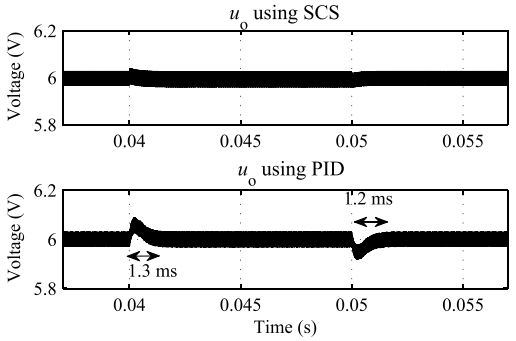


Fig. 12. Simulation results of output voltage response to the input voltage changes (15 V → 18 V → 12 V) for buck converter B working in DCM.

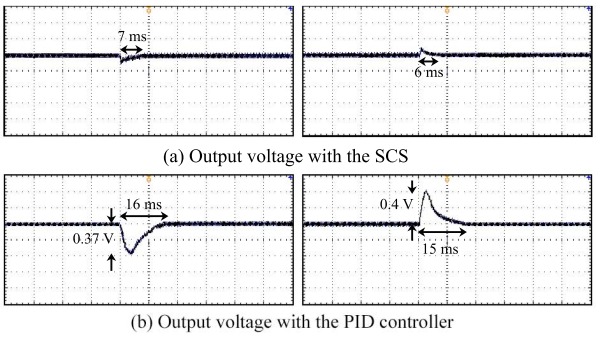


Fig. 13. Experimental results of output voltage response to the load current step changes (8 Ω → 4 Ω → 8 Ω) for buck converter A working in CCM (X_{axis}: 10 ms/div; Y_{axis}: 200 mV/div).

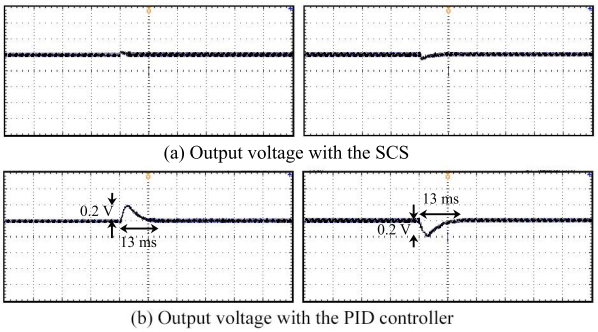
A prototype is constructed in order to experimentally test the SCS. In the experiment, the voltage and current measurements are made using CHV-25P and CHB-25NP/6 A,

TABLE II
SIMULATION RESULTS OF BUCK CONVERTER B IN ALL THE DYNAMIC CASES

disturbance (R or u_{in})	SCS		PID	
	Δu_o	$t_{settling}$	Δu_o	$t_{settling}$
8 Ω → 4 Ω → 8 Ω (CCM)	-0.05 V / 0.1 V	0.5 ms /0.3 ms	-0.3 V /0.2 V	1.8 ms /1.8 ms
15 V→ 18 V → 12 V (CCM)	0.01 V / -0.03 V	0.1 ms / 0.4 ms	0.08 V / -0.2 V	0.8 ms / 1.6 ms
8 Ω → 4 Ω → 8 Ω (DCM)	-0.05 V / 0 V	0.2 ms / 0.5 ms	-0.22 V / 0.21 V	1.9 ms / 1.4 ms
15 V→ 18 V → 12 V (DCM)	0.03 V / -0.01 V	0.3 ms / 0.2 ms	0.08 V / -0.08 V	1.3 ms / 1.2 ms

TABLE III
EXPERIMENTAL RESULTS OF BUCK CONVERTER A IN ALL THE DYNAMIC CASES

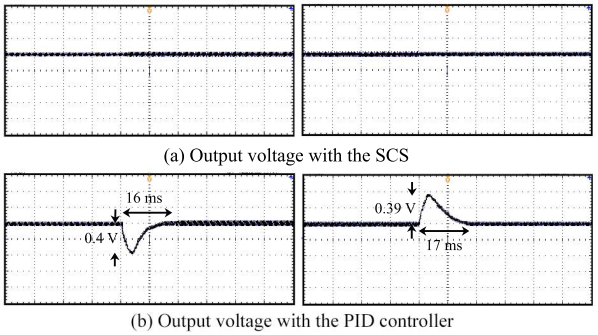
disturbance (R or u_{in})	SCS		PID	
	Δu_o	$t_{settling}$	Δu_o	$t_{settling}$
8 Ω → 4 Ω → 8 Ω (CCM)	-0.2 V / 0.0 V	7 ms / 6 ms	-0.35 V / 0.4 V	16 ms / 15 ms
15 V→ 18 V → 12 V (CCM)	0.01 V / -0.02 V	3 ms / 2 ms	0.2 V / -0.2 V	13 ms / 13 ms
8 Ω → 4 Ω → 8 Ω (DCM)	0 V / 0 V	0 ms / 0 ms	-0.4 V / 0.39 V	16 ms / 17 ms
15 V→ 18 V → 12 V (DCM)	0.04 V / 0.03 V	3 ms / 4 ms	0.25 V / -0.15 V	17 ms / 16 ms



(a) Output voltage with the SCS

(b) Output voltage with the PID controller

Fig. 14. Experimental results of output voltage response to the input voltage step changes (15 V → 18 V → 12 V) for buck converter A working in CCM (X_{axis}: 10 ms/div; Y_{axis}: 200 mV/div).

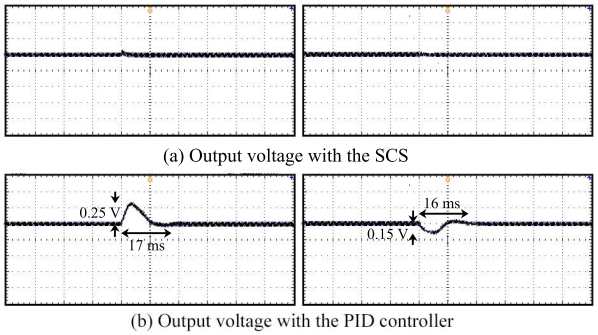


(a) Output voltage with the SCS

(b) Output voltage with the PID controller

Fig. 15. Experimental results of output voltage response to the load current step changes (8 Ω → 4 Ω → 8 Ω) for buck converter A working in DCM (X_{axis}: 10 ms/div; Y_{axis}: 200 mV/div).

respectively, and sent to dSPACE DS1104 controller. The IGBT gate drivers are based on SKYPER 32R which are powered with 0/15 V. All the experimental results are completed under the same conditions. Since the maximum sampling step (2×10^{-5} s) of the DS1104 limits the switching frequency of the system, buck converter A is constructed with



(a) Output voltage with the SCS

(b) Output voltage with the PID controller

Fig. 16. Experimental results of output voltage response to the input voltage step changes (15 V → 18 V → 12 V) for buck converter A working in DCM (X_{axis}: 10 ms/div; Y_{axis}: 200 mV/div).

the parameters identical to that of the simulation model in our experimental test bench. Experimental results presented thereafter are obtained from the oscilloscope (Tektronix) directly.

Figs. 13–16 show the experimental results of buck converter A working in CCM and DCM undergoing the step changes of the input voltage and the load current, respectively. The comparison results of the voltage shoot and settling time under all the dynamic cases are summarized in Table III. It can be observed from the figures and table that the experimental results are consistent with the simulation results. Significant dynamic performance improvements are observed.

VII. CONCLUSION

The SCS is based on the energy conservation principle in circuit and it has been designed and implemented to control buck converters. The SCS is capable of operating in both CCM and DCM. And it has a simple structure, which can be easily implemented. Furthermore, the stability of the converter controlled by the SCS has been proved using Lyapunov stability criterion. The dynamic response to

a positive load current step change demonstrates the SCS has superior dynamic performances.

Simulation and experimental results show that compared with the PID controller, the SCS produces superior dynamic performance, in terms of smaller voltage shoots and shorter settling times under the step changes of input voltage and load current. These results demonstrate that the SCS can be a substitute for classic controllers in power converter applications where a quick dynamic response is required. In addition, the SCS is here discussed for the buck converters and it can be easily extended to other converter topologies, such as boost converters, buck-boost converters and even inverters, which will be reported in the future.

REFERENCES

[1] A. Soto, P. Alou, J. A. Oliver, J. A. Cobos, and J. Uceda, "Optimum control design of PWM-buck topologies to minimize output impedance," in *Proc. 17th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2002, pp. 426–432.

[2] S. C. Huerta, A. Soto, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "Advanced control for very fast dc-dc converters based on hysteresis of the C_{out} current," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 1052–1061, Apr. 2013.

[3] C. Song and J. L. Nilles, "Accuracy analysis of hysteretic current-mode voltage regulator," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2005, pp. 276–280.

[4] L. Corradini, E. Orietti, P. Mattavelli, and S. Saggini, "Digital hysteretic voltage-mode control for dc–dc converters based on asynchronous sampling," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 201–211, Jan. 2009.

[5] M. J. Jafarian and J. Nazarzadeh, "Time-optimal sliding-mode control for multi-quadrant buck converters," *IET Power Electron.*, vol. 4, no. 1, pp. 143–150, Jan. 2011.

[6] B. R. Jo, H. W. Ahn, and M. J. Youn, "Multi-variable sliding mode control of quantum boost SRC," *IEEE Trans. Control Syst. Technol.*, vol. 2, no. 2, pp. 148–150, Jun. 1994.

[7] S. Oucheriah and L. P. Guo, "PWM-based adaptive sliding-mode control for boost dc–dc converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3291–3294, Aug. 2013.

[8] K. M. Smedley and S. Ćuk, "One-cycle control of switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 625–633, Nov. 1995.

[9] D. Yang, M. Yang, and X. Ruan, "One-cycle control for a double-input dc/dc converter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4646–4655, Nov. 2012.

[10] Y. Qiu, X. Chen, and H. Liu, "Digital average current-mode control using current estimation and capacitor charge balance principle for dc–dc converters operating in DCM," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1537–1545, Jun. 2010.

[11] E. Meyer, Z. Zhang, and Y.-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1802–1812, Jul. 2008.

[12] G. Feng, E. Meyer, and Y.-F. Liu, "A new digital control algorithm to achieve optimal dynamic performance in dc-to-dc converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1489–1498, Jul. 2007.

[13] H. C. Foong, Y. J. Zheng, Y. K. Tan, and M. T. Tan, "Fast-transient integrated digital dc-dc converter with predictive and feedforward control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1567–1576, Jul. 2012.

[14] A. Barrado, J. Quintero, A. M. Roldan, C. Fernández, P. Zumel, and E. Olias, "Linear-non-linear control applied in multiphase VRM," in *Proc. IEEE 36th Power Electron. Specialists Conf. (PESC)*, Jun. 2005, pp. 904–909.

[15] P. Gupta and A. Patra, "Hybrid mode-switched control of dc-dc boost converter circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 11, pp. 734–738, Nov. 2005.

[16] Y. Berkovich and A. Ioinovici, "Analysis and design of PWM regulators for large-signal stability," in *Proc. IEEE Int. Symp. Circuits Syst. ISCAS*, May 2002, pp. III-409–III-412.

[17] P. Gupta and A. Patra, "A stable energy-based control strategy for dc-dc boost converter circuits," in *Proc. IEEE 35th Annu. Power Electron. Specialists Conf.*, Jun. 2004, pp. 3642–3646.